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10/080,586	02/25/2002	Yasutoshi Aibara	XA-9625	8708

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EXAMINER

GLASS, CHRISTOPHER W

ART UNIT	PAPER NUMBER
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2878

DATE MAILED: 05/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/080,586

Applicant(s)

AIBARA ET AL.

Examiner

Christopher W. Glass

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 February 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 February 2002 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Abstract

1. The abstract of the disclosure is objected to because its awkward syntax and grammar preclude a clear understanding of the subject matter being described. Correction is required. See MPEP § 608.01(b).

Drawings

2. Figure 10 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. A substitute specification in proper idiomatic English and in compliance with 37 CFR 1.52(a) and (b) is required. The substitute specification filed must be accompanied by a statement that it contains no new matter.

4. The disclosure is objected to because of the following informalities: the specification, including the abstract, is replete with errors. Examples are as follows.

On line 2 of page 1, "the imaging system" should be replaced by "an imaging system".

On line 16 of page 1 (also on lines 7 and 11 of page 23), "DSP30" should read "DSP 30".

On lines 26 and 27 of page 2, "is also propagated also to" is grammatically incorrect.

On lines 15 and 16 of page 3, "and moreover only the pass-capacitor cannot remove the noise sufficiently" is unclear.

On line 18 of page 4, "Outline of" should be changed to read "An outline of".

On line 25 of page 4, "In more practical," could read "In more practical terms."

The sentence contained in lines 24-26 of page 12 is completely unclear in terms of what operation is being described.

Appropriate correction is required.

Claim Objections

5. Claims 1,5,9, and 11 are objected to because of the following informalities:

In line 8 of claim 1, "mans" should read "means".

In line 13 of claim 5, line 4 of claim 9, and line 4 of claim 11, it appears that "image process" should be changed to "image processing".

Appropriate correction is required.

6. There is insufficient antecedent basis for the following limitations in the claims: Claim 2 recites the limitations "the input binary code" and "the gray code" in line 4; Claim 3 recites the limitation "the input code" in line 4; Claim 4 recites the limitation "the input code" in lines 6-7; Claim 6 recites the limitation "the binary code" in line 6; Claim 8 recites the limitation "the input code" in line 6. For examination purposes, the limitations of claim 2 will be interpreted as though they read "an input binary code to a gray code"; "the input code" of claims 3 and 4 will be interpreted as referring to the input binary code mentioned in line 4 of claim 2; "the binary code" in claim 6 will be interpreted as if it read "binary code"; "the input code" in claim 8 will be interpreted as meaning "an input code".

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 5-9 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In lines 13-16, "including a second code conversion means for converting the codes outputted from said semiconductor integrated circuit device and an image processing circuit" is unclear as to whether codes from an image processing circuit are also converted, or if "and an image processing circuit" refers to another means included as part of the semiconductor integrated circuit device of line 12. For examination purposes, it will be assumed that the first interpretation was intended. Claims 6-9 and 11 are indefinite due to their dependence upon claim 5.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1 and 3 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,748,235 to Kondo et al. (hereafter Kondo). Figure 3 shows a semiconductor integrated circuit device comprising an amplifying circuit **4** for amplifying an analog color video signal outputted from an imaging element **3**, an A/D conversion circuit **5** for converting the amplified signal to a digital signal, a differential means **80** for obtaining a difference between the codes of

the adjacent pixels in regard to the same color after the A/D conversion (see Column 3, lines 35-47 and Column 5, lines 49-58) and a code conversion means **81,82**, composed of a circuit for adding or subtracting a fixed value to or from the input code (see Column 5, line 59 - Column 6, line 7), for code conversion of an output of the differential means.

11. Claim 10 is rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,515,698 to Sasaki et al. (hereafter Sasaki). In the means of Sasaki, a difference between the codes of the adjacent pixels in regard to the same color after the A/D conversion of the video signal by the A/D conversion circuit (**59**, Figure 6) and an output code of the differential means (**61,85**) is converted to the code of less number of bits to be changed over among the preceding and succeeding codes (see discussions of operation of matrix circuits **61,85** in Column 4, line 66 - Column 6, line 24; see also operation discussion of matrix circuit **3** of Figure 1, Column 3, line 35 - Column 4, line 23).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

13. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo, in view of U.S. Patent No. 6,192,146 to Abe. The code conversion means of Kondo is not expressly taught as being a binary gray code conversion circuit for converting the input binary code to gray code. However, this type of code conversion is well known in the art. Abe discloses an image processing system having a dither processing unit **124** (Figure 3-1) which performs this type of

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operation (see Column 5, line 37 - Column 6, line 10; see also background in Column 1, lines 36-42). It would have been obvious to one having ordinary skill in the art at the time the invention was made to implement this code conversion of the binary code in the means **81,82** of Kondo, in order to produce the gray code levels, since this technique is well known in the art and would only require algorithmic computation.

14. Claims 4/1 and 4/3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo, in view of Sasaki. The differential means **80** of Kondo is not expressly disclosed as being composed of a delay circuit for delaying an output code of the A/D conversion circuit **5** and a subtraction means for obtaining a difference between the code delayed by the delay circuit and the input code, while the delay circuit is constructed to vary a delay time depending on the color arrangement of the input video signal. However, this is well known in the art of image processing. Sasaki discusses in Column 4, lines 2-24 the use of a delay line in accessing pixel data for matrix calculations in such a device (see also Figures 2 and 6 for entire device overview). It would have been obvious to one having ordinary skill in the art at the time the invention was made to configure the differential means **80** of Kondo to implement such processes, in order to optimally access and process the color data of the input signal.

15. Claim 4/2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo, in view of Abe, as applied to claim 2 above, and further in view of Sasaki. The differential means **80** of the modified device of Kondo is not expressly disclosed as being composed of a delay circuit for delaying an output code of the A/D conversion circuit **5** and a subtraction means for obtaining a difference between the code delayed by the delay circuit and the input code, while the delay circuit is constructed to vary a delay time depending on the color arrangement of the input video

signal. However, this is well known in the art of image processing. Sasaki discusses in Column 4, lines 2-24 the use of a delay line in accessing pixel data for matrix calculations in such a device (see also Figures 2 and 6 for entire device overview). It would have been obvious to one having ordinary skill in the art at the time the invention was made to configure the differential means **80** of the modified device of Kondo to implement such processes, in order to optimally access and process the color data of the input signal.

16. Claims 5,7, 8/5, 8/7, 9/5, 9/7, 11/8/5, and 11/8/7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo, in view of Sasaki.

Regarding claims 5 and 7: Kondo shows in Figure 3 an imaging system comprising an imaging element **3** provided with a color filter **2**. Also disclosed is a semiconductor integrated circuit device comprising an amplifying circuit **4** for amplifying an analog color video signal outputted from an imaging element **3**, an A/D conversion circuit **5** for converting the amplified signal to a digital signal, a differential means **80** for obtaining a difference between the codes of the adjacent pixels in regard to the same color after the A/D conversion (see Column 3, lines 35-47 and Column 5, lines 49-58) and a first code conversion means **81,82**, composed of a circuit for adding or subtracting a fixed value to or from the input code (see Column 5, line 59 - Column 6, line 7), for code conversion of an output of the differential means. Kondo does not show a second code conversion means for converting the codes outputted from the semiconductor integrated circuit device and an image processing circuit, and wherein this second means is composed of a circuit for subtracting or adding a fixed value from or to an input code. However, Sasaki shows in Figures 2 and 6 an imaging system having second code conversion means **66-68** (**67** and **68** are digital-analog signal converters) and **73** after the differential means **61,85** (Figure

6), and which comprises means **73** for subtracting or adding a fixed value from or to an input code. It further would have been obvious to one having ordinary skill in the art to provide means such as the conversion means **66-68,73** of Sasaki in the device of Kondo, in order to process and convert the binary signal after it has been processed by the differential means **80** and first conversion means **81,82**, such that it can be reconverted to analog form and displayed or further processed in this form.

Regarding claims 8/5 and 8/7: The differential means **80** of Kondo is not expressly disclosed as being composed of a delay circuit for delaying an output code of the A/D conversion circuit **5** and a subtraction means for obtaining a difference between the code delayed by the delay circuit and the input code, while the delay circuit is constructed to vary a delay time depending on the color arrangement of the input video signal. However, this is well known in the art of image processing. Sasaki discusses in Column 4, lines 2-24 the use of a delay line in accessing pixel data for matrix calculations in such a device (see also Figures 2 and 6 for entire device overview). It would have been obvious to one having ordinary skill in the art at the time the invention was made to configure the differential means **80** of Kondo to implement such processes, in order to optimally access and process the color data of the input signal.

Regarding claims 9/5, 9/7, 11/8/5, and 11/8/7: Kondo does not expressly disclose the use of a storage means for storing digital video data, or the semiconductor integrated circuit device for image process as provided with a data compression circuit for compressing the code converted by a second code conversion means and a data expanding circuit for expanding the compressed data, wherein the data compressed by the data compression circuit is stored in the storage means. However, this is well known in the art, as taught by Sasaki. In the imaging

system shown by Figure 6 of Sasaki, "the digital values thus obtained (via A/D converter **59**) are sequentially stored in a memory **60**" and system controller **79** can read this data from the memory **60** (Column 5, lines 20-22). Sasaki also teaches that "data may of course be stored in a compressed form and reproduced in an expanded form" (Column 7, lines 5-6). It would have been obvious to one having ordinary skill in the art to utilize such a storage setup in the device of Kondo, such that digital data could be stored and later accessed for processing, and in which the data was compressed for storage and then expanded for use, in order to minimize the amount of memory space needed to store the data.

17. Claims 6, 8/6, 9/6, and 11/8/6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo, in view of Sasaki, as applied to claim 5 above, and further in view of Abe.

Regarding claim 6: The first and second code conversion means of the modified means of Kondo are not expressly taught as performing binary-gray conversion and gray-binary conversion, respectively. However, it is well known in the art to perform binary-gray and gray-binary code conversion through the use of a gray code conversion circuit, in such an imaging system. Abe discloses an image processing system having a dither processing unit **124** (Figure 3-1) which performs this type of operation (see Column 5, line 37 - Column 6, line 10; see also background in Column 1, lines 36-42). It would have been obvious to one having ordinary skill in the art at the time the invention was made to implement this code conversion of code in the (modified) means **81,82** of Kondo, in order to implement the gray code levels, and since this technique is well known in the art of image processing.

Regarding claim 8/6: The differential means **80** of the modified device of Kondo is not expressly disclosed as being composed of a delay circuit for delaying an output code of the A/D

conversion circuit **5** and a subtraction means for obtaining a difference between the code delayed by the delay circuit and the input code, while the delay circuit is constructed to vary a delay time depending on the color arrangement of the input video signal. However, this is well known in the art of image processing. Sasaki discusses in Column 4, lines 2-24 the use of a delay line in accessing pixel data for matrix calculations in such a device (see also Figures 2 and 6 for entire device overview). It would have been obvious to one having ordinary skill in the art at the time the invention was made to configure the differential means **80** of the modified device of Kondo to implement such processes, in order to optimally access and process the color data of the input signal.

Regarding claims 9/6 and 11/8/6: the modified device of Kondo does not expressly disclose the use of a storage means for storing digital video data, or the semiconductor integrated circuit device for image process as provided with a data compression circuit for compressing the code converted by a second code conversion means and a data expanding circuit for expanding the compressed data, wherein the data compressed by the data compression circuit is stored in the storage means. However, this is well known in the art, as taught by Sasaki. In the imaging system shown by Figure 6 of Sasaki, “the digital values thus obtained (via A/D converter **59**) are sequentially stored in a memory **60**” and system controller **79** can read this data from the memory **60** (Column 5, lines 20-22). Sasaki also teaches that “data may of course be stored in a compressed form and reproduced in an expanded form” (Column 7, lines 5-6). It would have been obvious to one having ordinary skill in the art to utilize such a storage setup in the modified device of Kondo, such that digital data could be stored and later accessed for processing, and in

which the data was compressed for storage and then expanded for use, in order to minimize the amount of memory space needed to store the data.

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

U.S. Patent No. 5,020,118 to Sugiura concerns an image reading apparatus, which shows in Figure 7 an image sensor array **201** connected to amplifying means **215,216**, A/D conversion means **217,218**, memory circuits **219,220**, and an image processing section **232**.

U.S. Patent No. 6,081,254 to Tanaka et al. discloses a color correction system of an imaging apparatus utilizing a sensor array of pixel elements and a display.

U.S. Patent No. 5,867,285 to Hirota et al. concerns a color image processor, having a delay memory in the digital-form image processing circuitry.

U.S. Patent No. 5,309,183 to Sasaki et al. shows in Figure 3 an image pickup and processing means comprising a sensor **101**, analog CDS processor **102**, sample/hold circuits **103**, differential amplifiers **107** amplifying the difference between pixel data obtained by the circuits **103**, an A/D converter **111** and a memory circuit **113** for storing the digital data.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher W. Glass whose telephone number is 703-305-1980. The examiner can normally be reached 9:30am-6:00pm, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Porta can be reached at 703-308-4852. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

cg
May 2, 2003


STEPHONE ALLEN
PRIMARY EXAMINER